RISC-V Processor

NOEL-ARTYA7-EX

NOEL-ARTYA7-EX Features

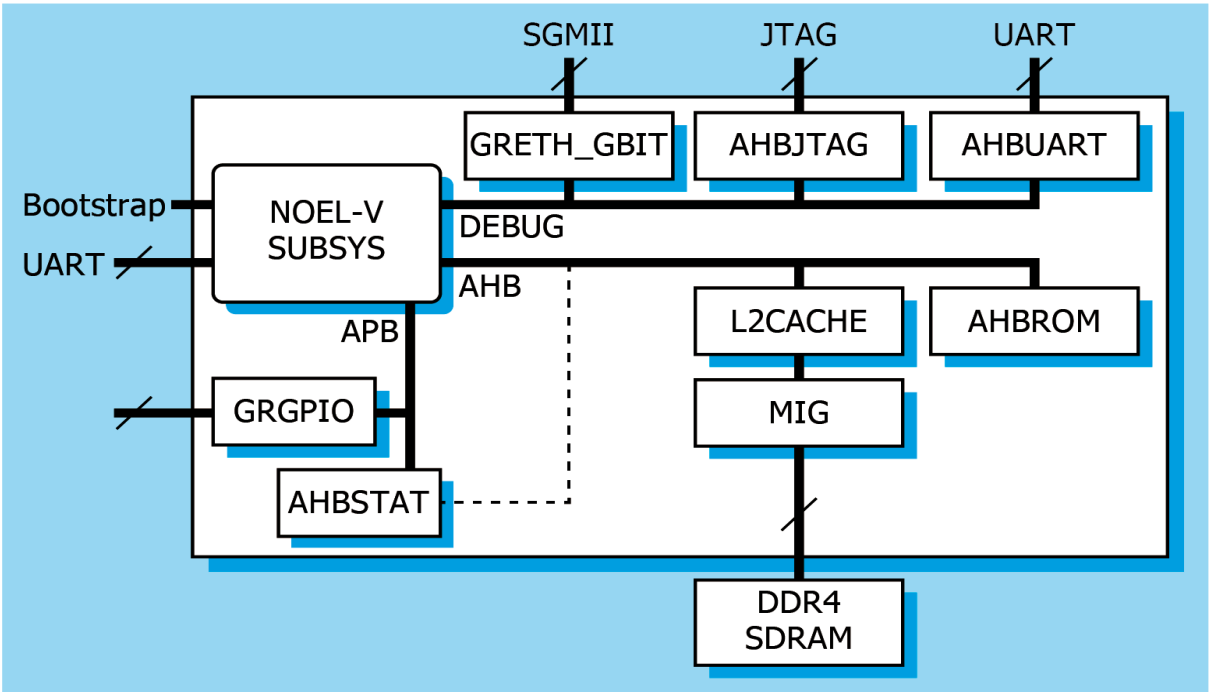
- RISC-V NOEL-V processor with 64-bit architecture 16 KiB instruction and 16 KiB data caches, memory management unit, hardware multiplier and divider, in single and multi-core configurations
- RISC-V standard Platform-Level Interrupt Controller
- RISC-V standard PMP
- RISC-V standard debug support
- Level-2 cache
- DDR4 SDRAM
- UART, Timers, GPIO port, Status registers
- Ethernet 10/100 Mbit MAC interface

Description

The NOEL-ARTYA7 FPGA bitstreams are a collection of example designs built from the GRLIB IP library using a template design for Xilinx Artix-7devices. The example designs are suitable for evaluation of NOEL microprocessors in system-on-chip designs.

Specification

- Targets Arty A7: Artix-7 FPGA Development Board (A7-100T version)



Applications

The NOEL/GRLIB template designs can be adapted as multiple configurations, covering instrument, payload and control applications.

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1 Introduction

1.1 Scope

The NOEL line of processors and the GRLIB IP library has support for Digilent Arty A7 board. This support consists of a techmap layer that wraps specific technology elements such as memory macros and pads. GRLIB also contains a template designs for developments boards such as the Digilent Arty A7 (A7-100T version) and infrastructure that automatically builds project files for Xilinx Vivado and synthesis tools such as Mentor Precision Hi-Rel and Synopsys Synplify Premier.

This document describes ready-made FPGA configurations (bitstreams) that have been built from a GRLIB template design.

More information about the NOEL-V processor is available at www.gaisler.com/NOEL-V

1.2 Document revision history

Table 1. Change record

Version	Date	Note
1.0	2020 December	First issue
1.1	2022 February	EX1 includes H extension. Other minor corrections.
2.0	2022 July	Updated example configurations
2.1	2022 December	Removed GP64L-SC example configuration
2.2	2023 May	Updated to Frontgrade branding

1.3 Reference documents

[AMBA] AMBA™ Specification, Rev 2.0, ARM IHI 0011A, 13 May 1999, Issue A, first release, ARM Limited

[GRLIB] GRLIB IP Library User's Manual, Frontgrade Gaisler, www.gaisler.com

[GRIP] GRLIB IP Core User's Manual, Frontgrade Gaisler, www.gaisler.com

[QSG] NOEL-ARTYA7-EX Quick Start Guide, NOEL-ARTYA7-EX-QSG, www.gaisler.com/NOEL-ARTYA7

2 Example designs

2.1 Overview

The NOEL-ARTYA7-EX example designs are based on a common architecture. The architecture is centered around the AMBA [AMBA] Advanced High-speed Bus (AHB), to which the processor(s) and other high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB) which is accessed through an AHB to APB bridge. The architecture for the basic design is shown in figure 1. Please also note that while not shown in the block diagram above, the Ethernet controller (GRETH) is also connected to the main AHB bus and not only the Debug AHB bus.

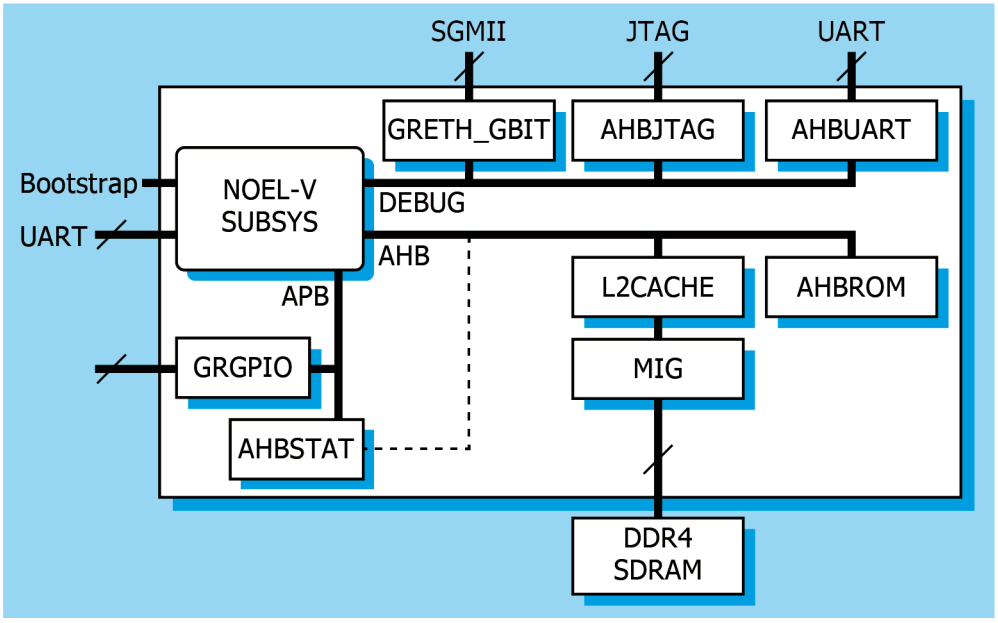

Figure 1. Architectural block diagram of NOEL-ARTYA7-EX

The full NOEL-ARTYA7 architecture includes the following modules:

- NOEL-V with 16 KiB instruction cache and 16 KiB data cache.
- Debug Support Unit with UART, Ethernet, and JTAG Debug Links
- Level-2 cache controller
- Xilinx MIG DDR3 SDRAM controller
- Timer unit with two 32-bit timers
- Platform-Level Interrupt Controller
- UART with FIFO and separate baud rate generator
- General purpose I/O port (GPIO).
- AMBA AHB status register

The GRLIB IP library contains a template design that has been used as the base for NOEL-ARTYA7-EX designs. The template design can easily be extended to add additional GRLIB IP library IP cores such as:

- Memory controllers with EDAC
- SpaceWire links with CRC support and hardware RMAP target
- SpaceFibre links
- Mil-Std-1553 BC/BM/RT

A full list of GRLIB IP library components can be found in [GRIP]. The GRLIB user's manual is available on-line [GRLIB].

2.2 Configurations

Table 2 below lists the NOEL-ARTYA7-EX example configurations. The bitstreams with example designs are intended to cover a wide range of application scenarios. Note that current available bitstreams have some limitations compared to the listed configuration.

The bitstreams are available for download from https://gaisler.com/NOEL-ARTYA7

Table 2. Example configurations

Configuration name	**MC32L-SC**	**GP32L-SC**	**MC64-SC**
Artix-7 device	**XC7A100T**	**XC7A100T**	**XC7A100T**
Processor	NOEL-V	NOEL-V	NOEL-V
RISC-V extensions*	RV64-IMA	RV32-IMACFD	RV64-IMCAFD
Memory Management Unit (MMU)	No	Yes	No
Number of processor cores	1	1	1
Level-1 cache	8+8 KiB	16+16 KiB	8+8 KiB
Hardware multiply&divide	Yes	Yes	Yes
Floating Point Unit	No	nanoFPU	nanoFPU
Physical Memory Protection (PMP)	Yes	Yes	Yes
Level-2 cache	Yes	Yes	Yes
UART Debug Link	Yes	Yes	Yes
JTAG Debug Link	Yes	Yes	Yes
Ethernet MAC 10/100 Mbit	Yes	Yes	Yes
Memory Controller	Xilinx DDR3 MIG & AHBROM	Xilinx DDR3 MIG & AHBROM	Xilinx DDR4 MIG & AHBROM
Standard peripherals	Yes	Yes	Yes

*Parts of the Bit manipulation and Encryption RISC-V extensions are also included. See NOEL-V section in GRLIB IP Core User's Manual for more details

Note: The configurations above are examples on how to use the GRLIB IP cores on ARTYA7. All IP cores have several configuration parameters and are individually configurable.

Note: The NOEL-V processor can be configured in several different standard configurations, including more RV32 variants, the configurations are listed at https://www.gaisler.com/NOEL-V

Note: While software may report that fault-tolerance is enabled for the example designs, the bitstreams are not suitable for use in harsh environments.

3 Architecture

3.1 Cores

The architecture is based on cores from the GRLIB IP library. The vendor and device identifiers for each core can be extracted from the plug & play information. The used IP cores are listed in table 3.

Table 3. Used IP cores

Core	Function	Vendor	Device
AHBCTRL	AHB Arbiter & Decoder	0x01	-
APBCTRL	AHB/APB Bridge	0x01	0x006
NOEL-V	NOEL-V RISC-V 64-bit processor	0x01	0xBD
RVDM	RISC-V Debug Module	0x01	0xBE
AHBUART	Serial/AHB debug interface	0x01	0x007
AHBJTAG	JTAG/AHB debug interface	0x01	0x01C
AHBSTAT	AHB failing address register	0x01	0x052
APBUART	8-bit UART	0x01	0x00C
GPTIMER	Modular timer unit with watchdog	0x01	0x011
GRETH	10/100 Mbit Ethernet MAC	0x01	0x01D
GRGPIO	General purpose I/O port	0x01	0x01A
L2CACHE	Level-2 Cache Controller	0x01	0x04B
Xilinx MIG	Xilinx DDR3 MIG - with GRLIB wrapper	0x01	0x090

3.2 Interrupts

The NOEL-ARTYA7-EX example designs use the same interrupt assignment for all configurations. See the description of the individual cores for how and when the interrupts are raised. All interrupts are handled by the interrupt controller and forwarded to the processor.

Table 4. Interrupt assignment

Core	Interrupt	Comment
AHBSTAT	4	
APBUART	1	
GPTIMER	2, 3	
GRETH_GBIT	5	

3.3 Memory map

The example designs use the same memory map for all standard configurations. The memory map shown in table 5 is based on the AMBA AHB address space. An access to addresses outside the

ranges will receive an AHB error response. The detailed register layout is defined in the description of each individual core.

Table 5. AMBA AHB address range

Core	Address range	Area
L2CACHE / PFDDR4	0x00000000 - 0x3FFFFFFF	DDR4 SDRAM area
AHBROM	0xC0000000 - 0xC001FFFF	Registers
CLINT	0xE0000000 - 0xE000FFFF	Registers
PLIC	0xF8000000 - 0xFBFFFFFF	Registers
GPTIMER	0xFC000000 - 0xFC0000FF	Registers
APBUART0	0xFC001000 - 0xFC0010FF	Registers
GRVERSION	0xFC080000 - 0xFC0800FF	Registers
AHBSTAT	0xFC080200 - 0xFC0830FF	Registers
GRGPIO	0xFC083000 - 0xFC0830FF	Registers
GRETH	0xFC084000 - 0xFC0840FF	Registers
AHBUART	0xFC086000 - 0xFC0860FF	Registers
Debug Module	0xFE000000 - 0xFEFFFFFF	Registers
L2CACHE IOAREA	0xFFF00000 - 0xFF3FFFFF	Registers
AHB plug&play	0xFFFFF000 - 0xFFFFFFFF	ROM area

3.4 IP core documentation

This user manual does not contain IP core documentation. Please refer to the GRLIB IP Core User's Manual [GRIP] available at http://gaisler.com/products/grlib/grip.pdf.

The GRMON debug monitor also provides information about the system-on-chip's configuration via the command **info sys**.

3.5 Signals

Please see the NOEL-ARTYA7-EX Quick Start Guide [QSG] for information on FPGA pinout.

3.6 Resource utilization

Resource utilization is described in the GRLIB area spreadsheet, available at:

https://www.gaisler.com/products/grlib/grlib_area.xls

4 Working with the board

4.1 Prerequisites

The following items are required to use NOEL-ARTYA7-EX designs:

- Workstation with Windows or Linux
- Arty A7: Artix-7 FPGA Development Board (A7-100T version)
- NOEL-ARTYA7 bitstream
- GRMON3 debug monitor

The two last items can be downloaded via http://gaisler.com/NOEL-ARTYA7.

Frontgrade Gaisler's standard offer of toolchains can be used to build and run software on the NOEL-ARTYA7-EX designs. Toolchains and run-time environments are available for download via http://gaisler.com.

4.2 Programming the FPGA device and connecting with GRMON3

Please see the NOEL-ARTYA7-EX Quick Start Guide [QSG] for information on FPGA programming and using the SoC design.

4.3 Support

In case of technical issues please contact support@gaisler.com. The support line is normally available only to companies and institutions with active support contracts. Limited support for the NOEL-ARTYA7-EX example designs is provided. When contacting support please provide a clear description of which design that is used and your affiliation.

Sales and licensing questions should be directed to sales@gaisler.com.

There is also an open forum available at https://grlib.community .

5 Ordering information

Please contact sales@gaisler.com for information on the GRLIB IP library.

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