

## **FTMCTRL: Failing SDRAM Access After Uncorrectable EDAC Error**

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Technical note

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Issue 1.0



## CHANGE RECORD

Issue	Date	Section / Page	Description
1.0	2015-10-27		First issue under this document name. This document replaces the document FTMCTRL-SDEDAC-ERR (latest released version was issue 1 revision 4).

## TABLE OF CONTENTS

1	OVERVIEW.....	3
1.1	Scope of the Document.....	3
1.2	Affected versions.....	3
1.3	Affected components.....	3
1.4	Distribution.....	3
1.5	Contact.....	3
2	DESCRIPTION.....	4
3	IMPACT.....	4
4	WORKAROUND.....	5
4.1	Workaround.....	5
4.2	Software versions with workaround.....	5
5	FAQ.....	5
5.1	I have tested error injection and have seen uncorrectable EDAC errors being handled correctly by my software. Does this mean that I am unaffected?.....	5
5.2	What happens if the second incoming access is to the PROM, SRAM or IO area?.....	5
5.3	Does the bug affect SRAM and PROM areas?.....	5
5.4	Will the controller always perform the unintended SDRAM read access when MCFG2.TRP=0?.....	5
5.5	I have a system with GRLIB build ID 4149 or later, am I affected by this bug?.....	6
5.6	How many clock cycles after the AMBA ERROR response does it take until the memory controller is back in normal state? .....	6
5.7	Is the unintended SDRAM access always a read operation?.....	6
5.8	Can this bug trigger for write operations? How about sub-word accesses with read-modify-write?.....	6

## **1 OVERVIEW**

### **1.1 Scope of the Document**

This document describes a bug present in the SDRAM controller of Aeroflex Gaisler's Fault-Tolerant Memory Controller (FTMCTRL) IP core where an AMBA access following an access that resulted in uncorrectable EDAC error may return erroneous data or an AMBA ERROR response.

The erratum is present in the SDRAM controller of FTMCTRL. FTMCTRL implementations that are implemented without SDRAM support and devices that do not make use of SDRAM are not affected.

### **1.2 Affected versions**

The errata is present in all FTMCTRL versions prior to GRLIB 1.3.9-b4149 that are implemented with SDRAM support.

### **1.3 Affected components**

Aeroflex components/products that are affected are:

- GR712RC
- LEON3-RTAX – versions with FTMCTRL with SDRAM support with a build ID lower than 4149.
- UT699, UT699E, UT700

### **1.4 Distribution**

LEON3FT users that have devices with the affected errata are free to use the material in this document in their own errata sheets. Contact Aeroflex Gaisler for inquires on other distribution.

### **1.5 Contact**

For questions on this errata, please contact Cobham Gaisler support at [support@gaisler.com](mailto:support@gaisler.com). When requesting support, include the part name if the question is a specific device or the full GRLIB IP library package name if the question relates to a GRLIB IP library license.

## 2 DESCRIPTION

When the memory controller detects an uncorrectable EDAC error it should respond with an AMBA ERROR response and then return to normal operation. Due to an incomplete condition check for starting new SDRAM accesses, the memory controller may perform a read access following an uncorrectable error even if there is no incoming access on the AMBA bus. The result will be discarded unless a AMBA read access to the SDRAM memory area is performed before the SDRAM read operation has finished. The extra read access will not occur if there is a SDRAM refresh operation pending.

The memory controller will return to normal operation after the extra read access has been performed. If a AMBA read is performed to the SDRAM area before this unintended read access has completed then the result of the incoming AMBA read access may be erroneous. The result can be an AMBA ERROR response or the memory controller may deliver data from the wrong memory location without a AMBA ERROR response (note that the first access that read a location which had an uncorrectable error will always receive an AMBA ERROR response).

The erratum can be triggered when:

- The FTMCTRL has been configured with minimum  $t_{RP}$  SDRAM timing, and
- A read access to SDRAM results in an uncorrectable EDAC error, and
- A second AMBA read access is performed to the SDRAM memory area in the window zero to five system clock cycles after the AMBA ERROR response given due to the uncorrectable EDAC error.

If the incoming read access occurs during the last cycle of the vulnerable window in time then the controller will return data from the memory location of the first access, which will may trigger an AMBA ERROR response if the uncorrectable error remains at that memory location. For incoming accesses during the other cycles in the vulnerable window, the access will malfunction but the data read by the memory controller may still have valid check bits. If the check bits are valid then the erroneous data will be delivered without any AMBA ERROR for the second access.

## 3 IMPACT

Uncorrectable SDRAM errors are expected to be a rare occurrence, provided that scrubbing of correctable errors has been implemented in the system. The uncorrected error response may be the result of a processor access which leads to the processor taking a trap. The read of the trap table may then occur during the window when the FTMCTRL performs the extra read access which leads to erroneous data or a AMBA ERROR response when the processor fetches the trap table. In multi-master systems, one master may trigger the uncorrectable error and a second master may perform a read access in the window where the FTMCTRL is malfunctioning. There are cases where the unintended read access is prevented. A SDRAM command issue or a refresh operation are cases that prevent triggering the erratum. It is recommended that all systems with FTMCTRL and SDRAM support implement the workaround described in the next section.

## 4 WORKAROUND

### 4.1 Workaround

The erratum cannot be triggered when the MCFG2.TRP field (bit 30 of MCFG2 register) is set to 1 (SDRAM  $t_{RP}$  parameter is three clock cycles).

### 4.2 Software versions with workaround

VxWorks board support packages for UT699, UT700 and GR712RC will be updated to default MCFG.TRP=1. For other boot loaders, please refer to the software package's documentation for information on how to set MCFG2.TRP.

GRMON2 will be updated to automatically set MCFG2.TRP for affected devices.

Please contact Cobham Gaisler support for information on specific software versions.

## 5 FAQ

### 5.1 **I have tested error injection and have seen uncorrectable EDAC errors being handled correctly by my software. Does this mean that I am unaffected?**

All FTMCTRL implementations with SDRAM support prior to 1.3.9-b4149 are affected. If MCFG2.TRP=1 is set in your system then you already have the workaround implemented and are unaffected by the erratum. Otherwise the timing of bus accesses in your test may have avoided triggering the bug but the erratum is still present and could potentially be triggered.

### 5.2 **What happens if the second incoming access is to the PROM, SRAM or IO area?**

Then the failure will not occur. The memory controller may perform the unintended read access to SDRAM but software will not be affected.

### 5.3 **Does the bug affect SRAM and PROM areas?**

No.

### 5.4 **Will the controller always perform the unintended SDRAM read access when MCFG2.TRP=0?**

Yes, unless there is a refresh operation pending.

**5.5 I have a system with GRLIB build ID 4149 or later, am I affected by this bug?**

No.

**5.6 How many clock cycles after the AMBA ERROR response does it take until the memory controller is back in normal state?**

Five system clock cycles.

**5.7 Is the unintended SDRAM access always a read operation?**

Yes.

**5.8 Can this bug trigger for write operations? How about sub-word accesses with read-modify-write?**

The bug does not trigger for write operations.

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