# GR-VPX-GR740

Quad Core LEON4FT Development Board for VPX

2020.11 Advanced Product Sheet

The most important thing we build is trust

GR-VPX-GR740 board with GR-VPX-SPW-MEZZ

GR-VPX-GR740 board without mezzanine

## Overview

With the GR-VPX-GR740 Development Board Cobham Gaisler introduces a high performance Single-Board Computer for use within OpenVPX and SpaceVPX environments.

Based on the Cobham Gaisler GR740 Quad-Core 32-bit LEON4FT SPARC V8 processor, the GR-VPX-GR740 comes in a 6U VPX format (233.5 mm x 160 mm) and is intended for use in OpenVPX chassis occupying a 1" slot (including mezzanine board). The board can also be used in stand-alone operation with a single 12V supply, in this case with limited VPX functionality.

The board is equipped with on-board memories for boot and application storage, and an SODIMM for SDRAM.

The front panel includes basic communication interfaces and LED indicators, whereas the rear connectors are intended for OpenVPX/SpaceVPX backplane connections.

The current GR-VPX-GR740 product includes a simple mezzanine board GR-VPX-SPW-MEZZ which provides two SpaceWire interfaces in the front panel. This mezzanine board do not include all the mezzanine interfaces provided by the main board.

The mezzanine interfaces supported by the main board are listed in this document and in the user manual to provide information for the users who can build their own mezzanine boards.

The main board supports the following mezzanine interfaces (which can be utilized by the users to build their own mezzanine cards):

A HPC-400 FMC connector for FPGA or other mezzanine boards provides interfaces with PCI, 2xSpaceWire and GPIO of the processor. It also connects to the Data Plane of the backplane via two Fat Pipes (8 differential pairs each) and four Thin Pipes (4 differential pairs each). Further signals routed between the mezzanine connector and the backplane include two Thin Pipes to the Control Plane and other system control signals. Among these mezzanine interfaces only the two SpaceWire interfaces are utilized by the GR-VPX-SPW-MEZZ and provided along with the delivered product.

Currently, this board product is not provided with any other mezzanine board other than the GR-VPX-SPW-MEZZ.

The board is developed to be used as a Switch Module in the OpenVPX architecture based on ANSI/VITA 65.0-2017 (GR-VPX-GR740-OX). It can also be ordered as a factory-configured variant with the backplane interface designed as a Switch and Controller Module providing some of the features of the SpaceVPX architecture specified in the Draft ANSI/VITA 78.00-2015 (GR-VPX-GR740-SX).

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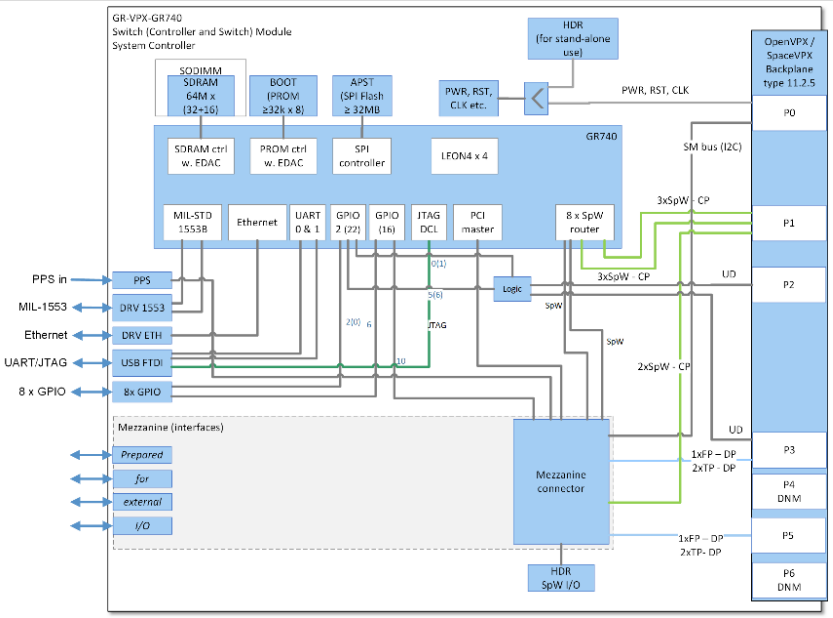
## Features

- Cobham Gaisler GR740 quad-core 32-bit fault-tolerant LEON4FT SPARC V8 processor
- On-board memory:
  - 256 MiB SODIMM SDRAM module for a total of 128 MiB accessible data RAM plus ECC check bits
  - Parallel Boot MRAM 128 KiB
  - SPI Flash memory 32 MiB
- Power, reset, clock and auxiliary circuits
- Interfaces at front edge of board:
  - MIL-STD-1553B Interface (Transceiver/Transformer and D-sub 9 Male connector)
  - RJ45 10/100/1000 Mbit GMII/MII Ethernet interface (KSZ9021GN)
  - 8-bit General purpose I/O (2x5 pin DIL header)
  - UART/JTAG interface using FTDI Serial to USB converter (FT4232HL with USB-Micro-AB)
  - PPS (Pulse Per Second) input for synchronization (SMB)
  - LED indicators for power, error, watchdog and PLL lock
  - Push button switch for reset
- Interfaces at the back edge of the board:
  - Supply and system control (VPX P0)
    - SM bus*
  - 8 SpaceWire interfaces (VPX P1)
    - six available from the main board GR740 SpW router
    - remaining two interfaced from the mezzanine connector*
  - User Defined (UD) signals from GPIO (VPX P2)
  - User Defined (UD) signals from GPIO (VPX P3)
  - 1 Fat Pipe and 2 Thin Pipes for high-speed serial data interfaces (VPX P3) *
  - 1 Fat Pipe and 2 Thin Pipes for high-speed serial data interfaces (VPX P5)*
- On-board mezzanine interface:
  - HPC-400 FMC connector
  - 2 SpaceWire interfaces connected to the GR740 router
  - 2 Thin Pipes routed to P1 on the back edge (used for 2 SpaceWire interfaces) *
  - 2 Fat Pipes and 4 Thin Pipes routed to P3 and P5 on the back edge*
  - 1 SpaceWire interface to on-board MDM9S connector*
  - SM bus*
  - PCI interface (32-bit) from the GR740*
  - 10-bit General Purpose I/O from the GR740*
  - Additional backplane clocks*
  - +12V supply
- Other interfaces on-board:
  - Input power connector for use without backplane: 12V nominal
  - SpaceWire connector for emulating backplane traffic (routed via mezzanine boards supporting this)
  - Assorted jumpers and test points for configuration and test
- Two factory-configured variants, the difference being related to pinout of the P1 connector for the Control Plane:
  - a) Part no GR-VPX-GR740-OX: OpenVPX, as per Switch Slot Profile SLT6- SWH-16U20F-10.4.2, compatible to backplane BKP6-CEN05-11.2.5.
  - b) Part no GR-VPX-GR740-SX: SpaceVPX, as per Switch and Controller Slot Profile SLT6-SWC-16T12F12U-10.4.1, compatible to backplane BKP6-CEN9-11.2.5 (not validated in a backplane).

**Note: These interfaces are available on the main board and interfaced with the mezzanine connector. Currently the mezzanine board delivered along with this product do not support and do not make use of these interfaces. These interfaces are listed to provide information for the users who can build their own mezzanine boards.*





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